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1. A circuit, comprising:

a logic circuit having a power input and a power return;

a capacitor coupled across the power input and the power return;

a first resistor having a first end coupled to the power input and a second end to couple to a power source; and

a second resistor having a first end coupled to the power return and a second end to couple to a power source return.

2. The circuit of claim 1 wherein the logic circuit comprises a differential circuit.

3. The circuit of claim 2 wherein the differential circuit comprises two logic gates.

4. (Amended) The circuit of claim 3 wherein the two logic gates are the same type of gate.

5. The circuit of claim 4 wherein the two logic gates each comprises an inverter.

6. The circuit of claim 5 wherein the two logic gates each further comprises complementary metal oxide semiconductor (CMOS) inverters.

7. (Amended) The circuit of claim 6 wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the power input, a gate, and a drain, and an n-channel transistor having a source coupled to the power return, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form an output node, the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output comprising the output nodes for each of the CMOS inverters.

8. (Amended) A circuit, comprising:

logic means for performing a logic function;

charge means for storing a charge across the logic means; and

isolation means for isolating the charge means from a power source.

9. The circuit of claim 8 wherein the charge means comprises a capacitor.

10. (Amended) The circuit of claim 9 wherein the isolation means comprises a first resistor to couple a first end of the capacitor to the power source, and a second resistor to couple a second end of the capacitor to a return line for the power source.

11. (Amended) The circuit of claim 8 wherein the logic means comprises a differential circuit.

12. The circuit of claim 11 wherein the differential circuit comprises two logic gates.

13. (Amended) The circuit of claim 12 wherein the two logic gates are the same type of gate.

14. The circuit of claim 13 wherein the two logic gates each comprises an inverter.

15. The circuit of claim 14 wherein the two logic gates each further comprises complementary metal oxide semiconductor (CMOS) inverters.

16. (Amended) The circuit of claim 15 wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the first end of the capacitor, a gate, and a drain, and an n-channel transistor having a source coupled to the second end of the capacitor, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form an output node, the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output comprising the output nodes for each of the CMOS inverters.

17. (Amended) A method of suppressing noise during the switching of a differential circuit having differential inputs and differential outputs, comprising:

charging a capacitor through a resistor;

applying a signal transition at the differential inputs; and

circulating charge between the differential outputs through the capacitor.

18. The method of claim 17 further comprising compensating for loss of the charge on the capacitor during the circulation of charge by recharging the capacitor through the resistor.

19. (Amended) The method of claim 18 further comprising clocking the differential circuit after a transition of the signal at the differential output, the circulation of the charge being initiated by clocking the differential circuit, the resistor and capacitor having a time constant that is less than half the clocking frequency.

20. An integrated circuit, comprising:
a differential circuit having a power input; and
an inductor having a first end coupled to the power input and a second end to couple to a power source.

21. The integrated circuit of claim 20 wherein the differential circuit further comprises a power return, the integrated circuit further comprising a second inductor having a first end coupled to the power return and a second end to couple to a power source return.

22. The integrated circuit of claim 20 wherein the inductor comprises a spiral inductor.

23. A circuit, comprising:
a differential circuit; and
a current source having an output coupled to the differential circuit, an input, and a capacitor shunting the input.

24. (Amended) The circuit of claim 23 wherein the current source comprises a transistor having a drain coupled to the differential circuit, a gate and a source, the capacitor being coupled between the gate and the source.

25. The circuit of claim 24 further comprising a bias circuit coupled to the gate of the transistor.

26. The circuit of claim 25 wherein the bias circuit comprises a resistor.